ABSTRACT OF THE DISCLOSURE

A semiconductor IC device includes, in a substrate, a P-type well region having a dynamic memory array section and applied with a reduced back bias voltage suitable for refreshing. Also included is a P-well region where N-channel MOSFETs of a peripheral circuit are formed. This P-well region is applied with a back bias voltage of an absolute value smaller than that applied to the P-type well of the memory array section. A P-type well section, where there are formed N-channel MOSFETs of an input circuit or an output circuit connected with external terminals, is applied with a back bias voltage of an absolute value large enough to provide a measure of protection against undershoot, while the refresh characteristics are improved by reducing the leakage current between the source/drain region connected with a capacitor and the P-type well, to thereby raise the operation speed of the peripheral circuit.